The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ROBERT T. FULLER, CHRIS MCCARTY, JOHN T. GASNER, and MICHAEL D. CHURCH

_____

Appeal No. 1998-2924
Application No. 08/276,290

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ON BRIEF

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Before FLEMING, RUGGIERO and GROSS, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 3-29, 31 and 32, all the claims pending in the application. Claims 1, 2 and 30 are canceled.

The instant invention relates to a method of manufacturing an improved BiCMOS semiconductor device. Specifically, the invention is directed to a complementary metal oxide semiconductor (CMOS) memory architecture in which an auxiliary bipolar transistor structure is formed in a well region that is formed in common with a CMOS memory cell. Appellants' specification ("specification"), page 1, lines 1-7. The auxiliary bipolar transistor structure is provided for the purpose of supplying a large magnitude current to enable programming of the memory cell. Specification, page 1, lines 15-20 to page 2, lines 1-4. The large current forced through the fusible links of a memory cell melts the fuse, severs the links, and forces the memory cell into a prescribed binary (1/0) condition. Specification, page 1, line 20 to page 2, line 4. The invention features the use of a separate implant mask for the emitter region of the auxiliary bipolar transistor. During the separate emitter formation step, the remainder of the substrate is masked, so that the emitter implant affects only the characteristics of the bipolar device. Specification, page 5. The geometry and impurity

concentration profile of the emitter region is tailored so that the auxiliary transistor has sufficient current gain to blow the fuse. Specification, page 4. Meanwhile, the doping parameters of the source/drain regions of the CMOS structure are separately established to maintain the integration density of the memory and prevent thyristor latch-up. Specification, page 4. During the implantation of the source/drain regions in the CMOS well region, the well region in which the auxiliary bipolar transistor is formed, is masked, so that no emitter region is formed in the well region used for the auxiliary bipolar transistor. Specification, page 5.

Appellants' independent claim 3, reproduced below, is representative:

3. A method of manufacturing a semiconductor architecture comprising the steps of:

(a) providing a semiconductor substrate of a first conductivity type having a first surface;

(b) forming, to a first depth from said first surface in respective first and second spaced-apart portions of said semiconductor substrate, first and second well regions of second conductivity type;

(c) forming first source and drain regions of said first conductivity type of a first channel conductivity type MOS structure in spaced apart surface portions of said first well

region, said first source and drain regions having a first doping and a second depth from said first surface, less than said first depth; and

(d) forming an emitter region of said first conductivity type of a bipolar transistor structure in said second well region, said second well region forming the base region of said bipolar transistor structure and said substrate forming the collector region of said bipolar transistor structure, such that said emitter region has a second doping greater than that of said first source and drain regions, and a third depth from said first surface deeper than said second depth of said first source and drain regions said first MOS structure.

In rejecting Appellants' claims, the Examiner relies on Appellants' admitted prior art in Appellants' Specification and Figure 1 and the following two other listed references:

Sagara et al. (Sagara) 5,118,633 Jun. 2, 1992

Tanabe et al. (Tanabe) EP 0,320,273 Jun. 14, 1989 (European Patent Application)

Claims 3-29, 31 and 32 stand rejected under 35 U.S.C. § 103 as being obvious over the combination of Appellants' admitted prior art and Tanabe et al. ("Tanabe") and Sagara et al. ("Sagara"). Rather than repeat the arguments of Appellants and Examiner, we refer the reader to the

Appellants' Brief[1] and Examiner's Answer[2] for the respective details thereof.

OPINION

With full consideration being given the subject matter on appeal, the Examiner's rejection and the arguments of Appellants and Examiner, for the reasons stated infra, we will affirm the Examiner's rejection of claims 3, 4, 7, 8, 11, 24, 25 and 28 under 35 U.S.C. § 103 as being unpatentable over the combination of Appellants' admitted prior art, Tanabe and Sagara. We will reverse the Examiner's rejection of claims 5, 6, 9, 10, 12-23, 26, 27, 29, 31 and 32.

Before consideration of Appellants' substantive arguments, we first address procedural matters related to Appellants' claim grouping. Initially, on page 28 of the

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[1] Appellants filed an Appeal Brief ("Brief") on December 29, 1997.

[2] The Examiner, in response to Appellants' Brief, filed an Examiner's Answer on March 17, 1998.

Brief, Appellants group together claims 3-9, 11, 24, 25 and 28. Then, in Argument, Appellants argue claims 3, 7, 11, and 25 together and claim 5 separately. Rule 37 CFR § 1.192(c)(7) sets forth the requirements for claim grouping. It states:

> *Grouping of claims*. For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

July 1, 1996, ***as amended at*** 60 Fed. Reg. 14518 (March 17, 1995).

Based on this Rule, we treat claims 3, 4, 7, 8, 11, 24, 25 and 28 as standing or falling together and select claim 3 as the representative claim of this group. We treat claims 5 and 9 separately.

Turning now to Appellants' arguments, we focus first on the arguments related to claim 3.

Appellants state that "the Examiner alleges that the admitted prior art of [Appellants'] Figure 1 discloses substantially the claimed process of forming first and second well regions having the same depth." Brief, page 30. Next, Appellants argue that it can be inferred from Tanabe that the depths of the respective base and well regions are not the same. Brief, page 31. Finally, Appellants argue that Sagara teaches away from forming a base well having the same depth as the well in which an adjacent MOS device was formed. Brief, page 32.

In response, the Examiner points out that Appellants' Figure 1 and the Background of the Invention illustrates base and well regions of the same depth. Examiner's Answer, page 3. The Examiner already asserted in the Final Rejection, Paper No. 17, that "[The] Background of the invention, pages 1-4 and related Fig. [figure] 1 discloses substantially the claimed process for forming a programmable CMOS memory device including the steps of forming first and second well regions having the same depth

. . . .” Now, the Examiner concludes that Appellants' limitation has "been clearly disclosed and admitted as Prior Art in the Background of the Invention." Examiner's Answer, page 4.

We find that Appellants' claim 3 limitation of "forming, to a first depth from said first surface in respective first and second spaced-apart portions of said semiconductor substrate, first and second well regions of second conductivity type" is taught by Appellants' admitted prior art as disclosed in Appellants' Specification, page 2, lines 5-16. This section of the Specification recites in part,

> A CMOS memory cell architecture . . . having a top surface 13, in respective first and second spaced portions 21 and 23 of which *P-type well regions 31 and 33 are formed to a prescribed depth* in substrate 11. (Emphasis added).

Specification, page 2, lines 1-12. Additionally, we find that Appellants' Figure 1 illustrates the well regions 31 and 33 having a same depth.

Appellants do not traverse or otherwise dispute the Examiner's contention that Appellants' admitted prior art does teach the depth limitation. Appellants only argue that Tanabe

and Sagara individually do not teach the depth limitation. Although we appreciate Appellants' argument that neither Tanabe nor Sagara teach that the depths of the respective base and well regions are the same, Appellants' argument is unpersuasive here where the Examiner relies solely on the admitted prior art for the rejection of this claim limitation and excludes the teaching of Tanabe and Sagara from consideration.

Next, Appellants argue that Tanabe contains no disclosure or suggestion of making the emitter region deeper and doping concentration greater than that of source and regions of a MOS device in a same depth well. Brief, page 32. Further, Appellants argue that Sagara discloses a method of manufacturing a BiCMOS device that is considerably different from that of either the prior art or Appellants' claims and emphasize that Sagara does not implant an emitter region but rather out diffuses it from a doped surface. Brief, page 33.

Our review of Sagara finds that Sagara teaches the claim limitation "forming an emitter region . . . such that said emitter region has . . . a third depth from said first surface

deeper than said second depth of said first source and drain regions [of] said first MOS structure." We base our finding on the following passage citations from Sagara: Sagara, at column 2, lines 30-35 discloses that ". . . source and drain regions of MOS transistors are formed after the formation of an emitter of a bipolar transistor, whereby a BiCMOS having the characteristic of xj(MOS)# xjE(Bip)# 0.15 µm can be formed easily." Additionally, Sagara, at column 3, lines 24-28 discloses, "Moreover, by satisfying the relation xj(MOS)# xjE(Bip)# 0.15 µm, it is possible to form an extremely fine MOS transistor and a high-performance bipolar transistor at a time." Finally, at column 3, line 44, Sagara discloses ". . . by satisfying the relation xj(MOS)# xjE(Bip)# 0.15 µm, attenuation and the improvement of integration density can be realized while maintaining xjE(Bip) to 0.15 µm or less.

Appellants argue that Sagara "does not implant the emitter region, but rather out diffuses it from a doped surface polycrystalline silicon layer." Brief, page 33. But this argument is neither persuasive nor dispositive here where

Appellants' claimed methodology includes neither diffusion nor implantation.

Furthermore, we find that Sagara teaches the claim limitation "forming an emitter region . . . such that said emitter region has a second doping greater than that of said first source and drain regions . . . ." Sagara discloses the greater doping concentration limitation at column 4, lines 33-37:

> Next an opening is formed in part of the silicon dioxide film, and an n+ -type polycrystalline silicon film *which contains a high concentration of impurity is formed therein*, followed by heat treatment at 900° C to form an n^+ type emitter. (emphasis added).

Sagara additionally discloses at column 4, lines 60-62, that Figure 8 illustrates "a sectional structure of a BiCMOS formed according to the present invention and having LDD (lightly doped drain) type MOS transistors" to support the argument that Sagara teaches Appellants' claimed limitation of an emitter region having a second doping greater than that of said first source and drain regions.

We note that Appellants do not contest the combinability of the prior art references. Although Appellants, on page 43 of Argument, assert that "the Examiner has failed to show where in the prior art . . . there is any teaching to combine the references . . .," Appellants do not further explain why the references, taken as a whole, do not suggest the claimed subject matter, nor do Appellants explain why features disclosed in one reference may not properly be combined with features disclosed in another reference.

Rule 37 CFR § 1.192 (c)(8)(iv) requires in part:

> If the rejection is based upon a combination of references, the argument shall explain why the references, taken as a whole, do not suggest the claimed subject matter, and shall include, as may be appropriate, an explanation of why features disclosed in one reference may not properly be combined with features disclosed in another reference. A general argument that all the limitations are not described in a single reference does not satisfy the requirements of this paragraph.

July 1, 1996, ***as amended at*** 60 Fed. Reg. 14518 (March 17, 1995). Appellants' assertions constitute general arguments that fail to satisfy the rule requirements.

Appellants' arguments only address the non-obviousness of the individual prior art references. However, "[n]on-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." ***In re Merck & Co., Inc.***, 800 F.2d 1091, 1098-99, 231 USPQ 375, 380. We are not required to now consider the issue of combinability. As stated, in part, by Rule 37 CFR § 1.192(a),

> The brief . . . must set forth the authorities and arguments on which appellant will rely to maintain the appeal. Any arguments or authorities not included in the brief will be refused consideration by the Board of Patent Appeals and Interferences, unless good cause is shown.

37 CFR § 1.192(a), revised, 62 CFR § 53131, Oct. 10, 1997, effective Dec. 1, 1997. In sum, by failing to argue combinability in the Brief, Appellants have effectively waived this argument as a consideration for appeal.

Our reviewing court further states in ***In re Baxter Travenol Labs***, 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991), "[i]t is not the function of this court to examine the claims in greater detail than argued by an appellant,

looking for nonobvious distinctions over the prior art." Just as our reviewing court does not, ***sua sponte***, raise or consider issues not argued, we are similarly not burdened to do the same.

Based on the foregoing, we find that the admitted prior art and Sagara teach all Appellants' claim 3 limitations. Because we find that the admitted prior art and Sagara read on Appellants' claims, we do not consider the Tanabe reference and affirm the Examiner's rejection of claim 3 based solely on the admitted prior art and Sagara references. We do not consider this to be a new ground of rejection. As ***In re Halley*** states, "[I]t is proper . . . to study the whole of the various references in the record and to apply one rather than a combination of two or three against the claims . . . ." ***In re Halley***, 296 F.2d 774, 778, 132 USPQ 16, 20 (CCPA 1961). ***See also In re Kronig and Scharfe***, 539 F.2d 1300, 1044, 190 USPQ 425, 426-427 (CCPA 1976).

Appellants have already acknowledged that claims 4, 7, 8, 11, 24, 25, and 28 stand or fall together with claim 3. Accordingly, we affirm the Examiner's rejection of claims 4,

7, 8, 11, 24, 25, and 28 as obvious over the admitted prior art and Sagara.

We now separately address claim 5. Appellants argue that the Examiner has failed to point to any portion of the cited prior art which correlates with the language of claim 5. Brief, page 34.

Claim 5 recites:

5. A method according to claim 4, wherein step (d) comprises selectively masking said first surface of said substrate so as to provide a third impurity introduction aperture overlying said second well region, introducing impurities of said first conductivity type at a second dosage energy to said third depth in said second well region, and introducing impurities of said first conductivity type at a third dosage energy to a fourth depth less than said third depth in said second well region.

We note that neither the admitted prior art, Tanabe nor Sagara teaches the limitations of claim 5. Specifically, as outlined on page 33 of the Brief, there exists no teaching for 1) "introducing impurities of a first conductivity type at a second dosage energy to a third depth in the second well, and (2) introducing impurities of the first conductivity type of the third dosage energy to a fourth depth less than the third depth in the second well region." Moreover, we also find no

suggestion in the prior art references to support the Examiner's rejection.

It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1,6 (Fed. Cir. 1983). The Examiner, having failed to point out any teachings or suggestions of the claim 5 limitations in the prior art, either alone or in combination, has not established a ***prima facie*** case. To establish a ***prima facie*** case of obviousness, the examiner must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. ***See In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598. Accordingly, we reverse the Examiner's rejection of claim 5 as obvious over the prior art. Appellants previously acknowledged that the patentability of claim 9 stands or falls with the patentability of claim 5. Brief, page 34. Therefore, we also reverse the Examiner's rejection

of claim 9 as obvious over the prior art. Claims 6 and 10 depend from claims 5 and 9, respectively, and the rejection of these claims are likewise reversed.

Considering now independent claim 14, Appellants argue that Sagara does not show a LOCOS field oxide having a bird's peak, and additionally does not disclose or suggest the spacing requirement of claim 14. Brief page 36. Appellants further argue that Tanabe also fails to show a LOCOS field oxide. The Examiner responds that Sagara illustrates the field oxide limitation at region 7 of figures 2-8, at region 24 of figures 13-16 and at region 49 of figure 18. Examiner's Answer, page 4. The Examiner points to Sagara's illustration of the field oxide region 49 in Figure 18 and equates the corner edge to a bird's beak (". . . in which the corner edge or bird's beak is spaced apart from emitter region . . .”). Examiner's Answer, pages 4-5.

Claim 14 recites:

14. A method of manufacturing a semiconductor architecture comprising the steps of:

(a) forming, in respective first and second spaced-apart portions of a semiconductor substrate of a first conductivity type, first and second well regions of a second conductivity to a first depth from a first surface of said substrate;

(b) forming a first channel conductivity type MOS structure formed in said first well region by introducing first source and drain regions of said first conductivity type in spaced apart surface portions of said first well region, such that said first source and drain regions have a first doping and a second depth from said first surface, less than said first depth;

(c) forming, in said second spaced-apart portion of said substrate including said second well region, a bipolar transistor structure having an emitter region of said first conductivity type, a base region of said second conductivity type and a collector region of said first conductivity type, such that said second well region forms said base region and said substrate forms said collector region;

(d) forming a second channel conductivity type MOS structure formed in said substrate by introducing second source and drain regions of said second type in spaced apart surface portions of said substrate adjacent to said first well region containing said first channel conductivity type MOS structure; and

(e) performing local oxidation of on the surface of said substrate to form a field oxide having an aperture therethrough overlying said second well region, such that a first 'bird's peak' edge of said aperture through said field oxide is spaced apart from said emitter region by a distance sufficient to prevent radiation incident upon said field oxide from initiating parasitic channel turn-on in surface portion of said second well region between said emitter region and said substrate.

Appellant's Specification defines "bird beak" as the reduced thickness portion of field oxide adjacent to the PN junction between P-well and substrate. Specification, page 14, lines 14-19. We find that Sagara does not teach or suggest a LOCOS field oxide having a bird's beak, as defined by Appellants' specification. Additionally, there is no teaching or suggestion in Sagara of a spacing requirement. Therefore, we reverse the Examiner's rejection of claim 14. Claims 15-18 depend from claim 14 and we likewise reverse the rejection of these dependent claims.

Dependent claim 12 incorporates a limitation similar to claim 14. Having already determined that Sagara does not teach or suggest the limitation of a LOCOS field oxide having a bird's beak or teach or suggest a spacing requirement limitation, we reverse the Examiner's rejection of claim 12. Claim 13, which depends from claim 12, is likewise reversed.

Turning now to independent claim 19, Appellants argue that neither the admitted prior art nor Tanabe teaches the limitation "that the field oxide does not overlie the first surface portion of the second well region between the emitter

region and the base contact region." Brief, page 37. Appellants further argue that Sagara does not disclose a LOCOS process to form the field oxide. Brief, page 38.

Claim 19, step (e) recites this limitation. It states,

> 19. (e) performing local oxidation of the surface of said substrate to form field oxide having an aperture therethrough overlying said second well region, such that said field oxide does not overlie said first surface portion of said second well region between said emitter region and said base contact region.

We find that neither the admitted prior art, nor Tanabe nor Sagara teaches Appellants' claim limitations as recited by claim 19, step (e), supra. Examiner has failed to establish a ***prima facie*** case. Accordingly, we reverse the Examiner's rejection of claim 19. Claims 20-23 depend from claim 19 and we likewise reverse the rejection of these dependent claims.

Considering now independent claim 29, Appellant argues that the cited prior art contains no teaching or suggestion of LOCOS formation of the field oxide, so that the bird's beak edge of the field oxide aperture is spaced apart from the emitter region. Brief, page 42.

Claim 29, step (d) recites this limitation as follows:

29. (d) performing local oxidation of the surface of said substrate to form a field oxide having an aperture therethrough overlying said second well region, such that a first 'bird's beak' edge of said aperture through said field oxide is spaced apart from said emitter region by a first surface portion of said second well region therebetween; and

We find that neither the admitted prior art, Tanabe, nor Sagara teaches or suggests, alone or in combination, the limitations of Appellants' claim 29, step (d). The Examiner has failed to establish a ***prima facie*** case. Therefore, we reverse the Examiner's rejection of claim 29. Claims 31 and 32 depend from claim 29 and we likewise reverse the rejection of these dependent claims.

Based on the foregoing, in summary, we affirm the rejection of claims 3, 4, 7, 8, 11, 24, 25 and 28 as unpatentable over the cited prior art under 35 U.S.C. § 103; we reverse the rejection of claims 5, 6, 9, 10, 12-23, 26, 27, 29, 31 and 32 under
35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

MICHAEL R. FLEMING Administrative Patent Judge	)
JOSEPH F. RUGGIERO Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

Appeal No. 1998-2924
Application NO. 08/276,290

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